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Claims

[c1] 1. A semiconductor structure, comprising:
an electrically conducting wire; and
first and second semiconductor regions being electrically coupled to the electrically conducting wire and being doped with first and second doping types, respectively, wherein the first and second doping types are of opposite doping types,
wherein without the second semiconductor region, in response to the first semiconductor region being excited and the electrically conducting wire being directly exposed to an ionic solution, a first current flows between the ionic solution and the first semiconductor region through the electrically conducting wire, and
wherein with the presence of the second semiconductor region, in response to the first semiconductor region being excited and the electrically conducting wire being directly exposed to the ionic solution, a second current flows between the first semiconductor region and the second semiconductor region so as to reduce the magnitude of the first current.

[c2] 2. The structure of claim 1, wherein the second semi-

conductor region is electrically coupled to the electrically conducting wire via the first semiconductor region.

[c3] 3. The structure of claim 1, wherein the first and second semiconductor regions are electrically coupled to each other via the electrically conducting wire.

[c4] 4. The structure of claim 1, wherein the first and second doping types are N and P types, respectively.

[c5] 5. The structure of claim 1, wherein the first and second doping types are P and N types, respectively.

[c6] 6. The structure of claim 1, wherein the second semiconductor region is inside the first semiconductor region.

[c7] 7. The structure of claim 1, wherein the second semiconductor region is outside the first semiconductor region.

[c8] 8. The structure of claim 1, wherein the first semiconductor region comprises a third semiconductor region being heavily doped with the first doping type, and wherein the first semiconductor region is electrically coupled to the electrically conducting wire via the third electrically conducting wire.

[c9] 9. The structure of claim 8, wherein the second semi-

conductor region is inside the first semiconductor region and is in physical contact with the third semiconductor region.

[c10] 10. The structure of claim 8, wherein the second semiconductor region is inside the first semiconductor region and is electrically coupled to the third semiconductor region via a conducting strap.

[c11] 11. A method for fabricating a semiconductor structure, the method comprising:

providing in the structure an electrically conducting wire, and first and second semiconductor regions being electrically coupled to the electrically conducting wire and being doped with first and second doping types, respectively, wherein the first and second doping types are of opposite doping types, and wherein without the second semiconductor region, in response to the first semiconductor region being excited and the electrically conducting wire being directly exposed to an ionic solution, a first current flows between the ionic solution and the first semiconductor region through the electrically conducting wire; and

in response to the first semiconductor region being excited and the electrically conducting wire being directly exposed to the ionic solution, generating a

second current between the first semiconductor region and the second semiconductor region so as to reduce the magnitude of the first current.

[c12] 12. The method of claim 11, wherein the second semiconductor region is electrically coupled to the electrically conducting wire via the first semiconductor region.

[c13] 13. The method of claim 11, wherein the first and second semiconductor regions are electrically coupled to each other via the electrically conducting wire.

[c14] 14. The method of claim 11, wherein the first and second doping types are N and P types, respectively.

[c15] 15. The method of claim 11, wherein the first and second doping types are P and N types, respectively.

[c16] 16. The method of claim 11, wherein the second semiconductor region is inside the first semiconductor region.

[c17] 17. The method of claim 11, wherein the second semiconductor region is outside the first semiconductor region.

[c18] 18. The method of claim 11, further comprising the step of providing a third semiconductor region in the first

semiconductor region, wherein the third semiconductor region is heavily doped with the first doping type, and wherein the first semiconductor region is electrically coupled to the electrically conducting wire via the third electrically conducting wire.

[c19] 19. The method of claim 18, wherein the second semiconductor region is inside the first semiconductor region and is in physical contact with the third semiconductor region.

[c20] 20. The method of claim 18, wherein the second semiconductor region is inside the first semiconductor region and is electrically coupled to the third semiconductor region via a conducting strap.

[c21] 21. A semiconductor structure, comprising:
a first semiconductor region doped with a first doping type; and
a first photo-blocking layer covered on top of the first semiconductor region and adapted for reducing light reaching and exciting the first semiconductor region.

[c22] 22. The structure of claim 21, further comprising an electrically conducting wire being electrically coupled to the first semiconductor region and being exposed to a manufacturing environment.

[c23] 23. The structure of claim 21, further comprising:a second semiconductor region doped with a second doping type, the first and second doping types being of opposite doping types; and
a second photo-blocking layer covered on top of the second semiconductor region and adapted for reducing light reaching and exciting the second semiconductor region.

[c24] 24. The structure of claim 23, further comprising an electrically conducting wire being electrically coupled to the second semiconductor region and being exposed to a manufacturing environment.

[c25] 25. The structure of claim 21, wherein the first photo-blocking layer comprises a silicide material.

[c26] 26. A method for identifying LMPF (Localized Metal Precipitate Formation) in a semiconductor structure, the method comprising:
providing in the semiconductor structure (a) a first electrically conducting wire, (b) a first semiconductor region doped with N type dopants and electrically coupled to the first electrically conducting wire, (c) a monitoring ramp terminal being near the first electrically conducting wire, electrically disconnected from the first electrically

conducting wire, and exposed to the atmosphere, and (d) a second electrically conducting wire;

applying a voltage difference to the monitoring ramp terminal and a select wire selected from the group consisting of the first and second electrically conducting wires; and

measuring a current flowing between the select wire and the monitoring ramp terminal so as to determine whether LMPF occurs at the first electrically conducting wire.

[c27] 27. The method of claim 26, further comprising the step of determining that LMPF occurs at the first electrically conducting wire if the measured current exceeds a prespecified value.

[c28] 28. The method of claim 26, wherein the second electrically conducting wire is electrically coupled to a second semiconductor region doped with P type dopants.

[c29] 29. The method of claim 26, wherein the selected wire is the first electrically conducting wire.

[c30] 30. The method of claim 26, wherein the selected wire is the second electrically conducting wire.

[c31] 31. The method of claim 26, further comprising the step of providing a second semiconductor region doped with

N+ type dopants, wherein the first semiconductor region is electrically coupled to the first electrically conducting wire via the second semiconductor region.

[c32] 32. The method of claim 26, wherein the ratio of a first area of the first semiconductor region to a second area of the first electrically conducting wire is between 100:1 and 750:1.

[c33] 33. A method for determining the sensitivity degree of a fabrication process performed on a wafer, the method comprising the steps of:
providing in the wafer a plurality of structures having various LMPF likelihood ratios;
monitoring LMPF at each of the plurality of structures and collecting monitoring data; and
determining the sensitivity degree of the fabrication process.

[c34] 34. The method of claim 33, wherein the step of monitoring LMPF at each of the plurality of structures comprises, for each of the plurality of structures,
applying a voltage difference to a monitoring ramp terminal and a wire in the structure; and
measuring a current flowing between the wire and the monitoring ramp terminal so as to determine whether the structure has LMPF.

[c35] 35. The method of claim 34, wherein the step of determining the sensitivity degree of the fabrication process comprises the step of determining the sensitivity degree of the fabrication process to be a value of an LMPF likelihood ratio where and above which the associated structures of the plurality of structures are determined to have LMPF.